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10/035,571	10/23/2000	Ryszard Bleszynski	40291/2000100	1452

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EXAMINER	
HAN, CLEMENCE S	

ART UNIT	PAPER NUMBER
2665	8

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,571	BLESZYNSKI ET AL.	
	Examiner	Art Unit	
	Clemence Han	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,23,24,29,30,37,39-41 and 48-50* is/are rejected.

7)☒ Claim(s) *21, 22, 25–28, 31–36, 38 and 42–47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. An initialed and dated copy of Applicant's IDS form 1449, Paper No. 2, is attached to the instant Office action.

Claim Objections

2. Claim 15 is objected to because of the following informalities: The phrase "particular one of the plurality of buffers" are repeated in line 8 and 9. Appropriate correction is required.

3. Claim 32 is objected to because of the following informalities: The term "write request queues" in line 12 should be "read request queues". Appropriate correction is required.

4. Claim 35 is objected to because of the following informalities: The term "an" in line 2 should be removed. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 1–20, 23, 24, 29, 30, 37, 39–41 and 48–50 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (US Patent 6,415,366).

In regarding to claim 1, Chen teaches a method to optimally access a memory unit where the memory unit is logically partitioned to form a plurality of memory channels, the plurality of memory channels are further logically partitioned to form a plurality of memory lines, each of the plurality of memory lines includes a plurality of buffers and each of the plurality of buffers corresponds to a separate one of the plurality of memory channels, comprising: determining at least one load value of each of the plurality of memory channels (Column 3 Line 56–62); and based on the determined at least one load value, selecting a particular one of the plurality of memory channels (Column 2 Line 36–39).

In regarding to claim 2, Chen teaches the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each of the plurality of memory channels, the number of pending read requests (Column 2 Line 39–43).

In regarding to claim 3, Chen teaches the step of selecting the particular one of the plurality of memory channels includes selecting the particular one of the plurality of memory channels that has a lowest number of pending read requests (Column 2 Line 39–43).

In regarding to claim 4, Chen teaches the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each of the plurality of memory channels, at least one of the number of pending write requests, and the number of active buffers which is the number of a particular one of the plurality of buffers that is unavailable and corresponds to the particular one of the plurality of memory channels in each of the plurality of memory (Column 3 Line 56–62).

In regarding to claim 5, Chen teaches the step of selecting the particular one of the plurality of memory channels includes selecting the particular one of the plurality of memory channels that has at least one of a lowest number of pending write requests, a lowest number of active buffers, and a corresponding channel identification number that is next in a round robin scheme (Column 2 Line 36–39).

In regarding to claim 6, Chen teaches the memory unit as a plurality of dynamic random access memory units (Column 3 Line 26–28).

In regarding to claim 7, Chen teaches each of the plurality of buffers having a fixed-size (Column 3 Line 10–25).

In regarding to claim 8, Chen teaches receiving an incoming information element; if the size of the information element is greater than the fixed-size of each of the plurality of buffers, dividing the information element into a plurality of

information element segments, each of the plurality of information element segments having a size less than or equal to the fixed-size of each of the at least one buffer (Column 3 Line 10–25); and storing at least one of the information element and a particular one of the plurality of information element segments within a particular one of the plurality of buffers corresponding to the selected one of the plurality of memory channels at a particular one of the plurality of memory lines (Column 3 Line 10–25).

In regarding to claim 9, Chen teaches each of the plurality of memory channels having a width equal to a width of the memory unit divided by the number of the plurality of memory channels (Figure 3, Column 3 Line 36).

In regarding to claim 10, Chen teaches a method to optimally access a memory unit where the memory unit is logically partitioned to form a plurality of memory channels, the plurality of memory channels are further logically partitioned to form a plurality of memory lines, each of the plurality of memory lines includes a plurality of buffers and each of the plurality of buffers corresponds to a separate one of the plurality of memory channels, comprising: determining at least one load value of each of the plurality of memory channels (Column 3 Line 56–62); and selecting a particular one of the plurality of memory channels that has

a particular one of the at least one load value that is the lowest (Column 2 Line 36–43).

In regarding to claim 11, Chen teaches the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each of the plurality of memory channels, at least one of the number of pending read requests, the number of pending write requests, and the number of active buffers which is the number of a particular one of the plurality of buffers that is unavailable and corresponds to the particular one of the plurality of memory channels in each of the plurality of memory lines (Column 3 Line 56–62).

In regarding to claim 12, Chen teaches the step of selecting the particular one of the plurality of memory channels that has the lowest determined load includes selecting the particular one of the plurality of memory channels that has at least one of a lowest number of pending read requests, a lowest number of pending write requests, a lowest number of active buffers, and a corresponding channel identification number that is next in a round robin scheme (Column 2 Line 36–39).

In regarding to claim 13, Chen teaches the memory unit as a plurality of dynamic random access memory units (Column 3 Line 26–28).

In regarding to claim 14, Chen teaches each of the plurality of buffers having a fixed-size (Column 3 Line 10–25).

In regarding to claim 15, Chen teaches receiving an incoming information element; if the size of the information element is greater than the fixed-size of each of the plurality of buffers, dividing the information element into a plurality of information element segments, each of the plurality of information element segments having a size less than or equal to the fixed-size of each of the at least one buffer (Column 3 Line 10–25); and storing at least one of the information element and a particular one of the plurality of information element segments within a particular one of the plurality of buffers corresponding to the particular one of the plurality of buffers to the selected one of the plurality of memory channels at a particular one of the plurality of memory lines (Column 3 Line 10–25).

In regarding to claim 16, Chen teaches each of the plurality of memory channels having a width equal to a width of the memory unit divided by the number of the plurality of memory channels (Figure 3, Column 3 Line 36).

In regarding to claim 17, Chen teaches a method to optimally access a single hierarchical level memory unit, where the memory unit is logically partitioned to form a plurality of memory channels, the plurality of memory channels are further logically partitioned to form a plurality of memory lines, each of the plurality of memory lines includes a plurality of buffers and each of the plurality of buffers

corresponds to a separate one of the plurality of memory channels, comprising: determining, for each of the plurality of memory channels, at least one of the number of pending read requests, the number of pending write requests, and the number of active buffers which is the number of a particular one of the plurality of buffers that is unavailable and corresponds to the particular one of the plurality of memory channels in each of the plurality of memory lines (Column 3 Line 56–62); and selecting a particular one of the plurality of memory channels that has at least one of a lowest number of pending read requests, a lowest number of pending write requests, a lowest number of active buffers, and a corresponding channel identification number that is next in a round robin scheme (Column 2 Line 36–39).

In regarding to claim 18, Chen teaches each of the plurality of buffers having a fixed-size (Column 3 Line 10–25).

In regarding to claim 19, Chen teaches receiving an incoming information element; if the size of the information element is greater than the fixed-size of each of the plurality of buffers, dividing the information element into a plurality of information element segments, each of the plurality of information element segments having a size less than or equal to the fixed-size of each of the at least one buffer (Column 3 Line 10–25); and storing at least one of the information element and a particular one of the plurality of information element segments

within a particular one of the plurality of buffers corresponding to the selected one of the plurality of memory channels at a particular one of the plurality of memory lines (Column 3 Line 10–25).

In regarding to claim 20, Chen teaches the single hierarchical level memory unit as a plurality of dynamic random access memory units (Column 3 Line 26–28).

In regarding to claim 23, Chen teaches upon storing at least one of the information element and the particular one of the plurality of information element segments within the particular one of the plurality of buffers corresponding to the selected one of the plurality of memory channels, setting a particular one of a plurality of payload channel occupancy bits that corresponds to the selected one of the plurality of memory channels (Column 4 Line 38–43).

In regarding to claim 24, Chen teaches reading the plurality of payload channel occupancy bits to determine if a corresponding one of the plurality of memory channels is available (Column 4 Line 38–43).

In regarding to claim 29, Chen teaches a system to optimally access a memory unit, comprising: the memory unit 20–27 that is logically partitioned to form a plurality of memory channels; a traffic analyzer 130 to determine at least one load of each of the plurality of memory channels; and a bandwidth balancer

120 to select a particular one of the plurality of memory channels based on the determined at least one load.

In regarding to claim 30, Chen teaches the plurality of memory channels of the memory unit are further logically partitioned to form a plurality of memory lines, each of the plurality of memory lines includes a plurality of buffers and each of the plurality of buffers corresponds to a separate one of the plurality of memory channels (Figure 3).

In regarding to claim 37, Chen teaches the memory unit as a plurality of dynamic random access memory units (Column 3 Line 26–28).

In regarding to claim 39, Chen teaches each of the plurality of buffers having a length that is a fixed-size (Column 3 Line 10–25).

In regarding to claim 40, Chen teaches each of the plurality of memory channels having a width that is the fixed-size (Column 3 Line 10–25).

In regarding to claim 41, Chen teaches a system to optimally access a memory unit, comprising: the memory unit 20–27 that is logically partitioned to form a plurality of memory channels; a bandwidth management unit that includes a traffic analyzer 130 to determine at least one load of each of the plurality of memory channels; and a bandwidth balancer 120 to select a particular one of the plurality of memory channels based on the determined at least one load; and a

policy control unit 140 to provide at least one of an information element and a particular one of a plurality of information element segments for writing to the selected one of the plurality of memory channels.

In regarding to claim 48, Chen teaches a program storage device readable by a computer system, storing a plurality of instructions to optimally access a memory unit where the memory unit is logically partitioned to form a plurality of memory channels, the plurality of memory channels are further logically partitioned to form a plurality of memory lines, each of the plurality of memory lines includes a plurality of buffers and each of the plurality of buffers corresponds to a separate one of the plurality of memory channels, comprising: instructions for determining at least one load value of each of the plurality of memory channels (Column 3 Line 56–62); and instructions for selecting a particular one of the plurality of memory channels based on the determined at least one load value (Column 2 Line 36–39).

In regarding to claim 49, Chen teaches the instructions for determining the at least one load value of each of the plurality of memory channels including instructions for determining, for each of the plurality of memory channels, at least one of the number of pending read requests, the number of pending write requests, and the number of active buffers which is the number of a particular one of the plurality of buffers that is unavailable and corresponds to the particular one of the

plurality of memory channels in each of the plurality of memory lines (Column 3 Line 56–62).

In regarding to claim 50, Chen teaches the instructions for selecting the particular one of the plurality of memory channels including instructions for selecting the particular one of the plurality of memory channels that has at least one of a lowest number of pending read requests, a lowest number of pending write requests, a lowest number of active buffers, and a corresponding channel identification number that is next in a round robin scheme (Column 2 Line 36–39).

Allowable Subject Matter

7. Claim 21, 22, 25–28, 31–36, 38 and 42–47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to the memory and the switch in general.

U.S. Patent 6,249,524 to Moriwaki et al.

U.S. Patent 5,649,217 to Yamanaka et al.

U.S. Patent 6,055,234 to Aramaki

U.S. Patent 5,539,747 to Ito et al.

U.S. Patent 3,702,006 to Page

U.S. Patent 4,633,387 to Hartung et al.

U.S. Patent 6,021,086 to Joffe

U.S. Patent 6,697,362 to Akella et al.

U.S. Patent 5,859,849 to Parks

U.S. Patent 5,394,397 to Yanagi et al.

U.S. Patent 6,510,161 to Trevitt et al.

U.S. Pub. 2001/0010692 to Sindhu et al.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (703) 305-0372. The examiner can normally be reached on Monday-Friday 8 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. H.

Clemence Han
Examiner
Art Unit 2665

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600